

CMOS Device and Method of Manufacture

ABSTRACT OF THE DISCLOSURE

A CMOS device and manufacturing method thereof wherein a bilayer etch stop is used over a PMOS transistor, and a single etch stop layer is used for an NMOS transistor, for forming contacts to the source or drain of the CMOS device. A surface tension-reducing layer is disposed between the source or drain region of the PMOS transistor and an overlying surface tension-inducing layer. The surface tension-inducing layer may comprise a nitride material or carbon-containing material, and the surface tension-reducing layer may comprise an oxide material. Degradation of hole mobility in the PMOS transistor is prevented by the use of the surface tension-reducing layer of the bilayer etch stop.